Abstract of the Disclosure

An input buffer circuit has a plurality of selectively enabled differential amplifier circuits, where each differential amplifier is configured for compatibility with a particular differential I/O standard and its corresponding input operating range. For example, the input buffer may have two differential amplifiers suitable for receiving LVDS differential input signals over a wide input operating range, and another differential amplifier suitable for receiving the PCML differential input signals. One or more control signals are provided to the input buffer, e.g., programmably, to selectively enable the required differential amplifier(s) for a given I/O standard.